AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims:

1. (currently amended) An address translation filter for filtering a signal on a system bus that couples between a core processor and an external memory unit, the address translation filter comprising:

a first interface operable under a first bus protocol to connect to the system bus and receive a virtual memory address from an external device connected to the bus;

a second interface operable under a second bus protocol to connect to the system bus and transmit a physical memory address to the external memory unit; and

an address translation unit, external to the core processor and coupled between the first and second interfaces, operable to determine the physical memory address from the virtual memory address,

wherein the first bus protocol is the same as the second bus protocol.

2. (original) An address translation filter in accordance with claim 1, wherein the address translation unit includes a lookup table indexed by virtual addresses.

3. (original) An address translation filter in accordance with claim 2, wherein the lookup table is indexed by the most significant portion of a virtual address.

4. (original) An address translation filter in accordance with claim 1, wherein the address translation unit comprises a translation lookaside buffer.

5. (original) An address translation filter in accordance with claim 4, further comprising:

a refresh logic unit operable to refresh the translation lookaside buffer when the virtual memory address is not matched by an entry in the translation lookaside buffer.

6. (previously presented) An address translation filter in accordance with claim 5, further comprising:

an output control link responsive to the refresh logic unit and operable to signal the core processor when the translation lookaside buffer is to be refreshed.

7. (original) An address translation filter in accordance with claim 5, further comprising:

an input for receiving an input system clock signal; and

an output for transmitting an output system clock signal,

wherein the output clock signal is paused while the translation lookaside buffer is being refreshed.

8. (original) An address translation filter in accordance with claim 1, wherein the virtual and physical memory addresses have the same width.

9. (currently amended) An integrated circuit ~~digital processing system~~, comprising:

a core processor;

~~an external memory unit;~~

~~an external~~ processing device external to the core processor;

an address translation filter; and

a system bus operable to link ~~linking~~ the core processor ~~the external memory~~ and the address translation filter to each other under a bus protocol and to link the ~~linking the external~~ processing device to the address translation filter under the same bus protocol,

wherein the address translation unit is operable to translate a virtual memory address received via the system bus from the ~~external~~ processing device into a physical memory address in an ~~transmitted via the system bus to the~~ external memory unit and to transmit the physical memory address to the external memory unit via the system bus.

10. (currently amended) An integrated circuit ~~digital processing system~~ in accordance with claim 9, wherein the address translation filter comprises:

a translation lookaside buffer; and

a refresh logic unit operable to refresh the translation lookaside buffer when the virtual memory address is not matched by an entry in the translation lookaside buffer.

11. (currently amended) An integrated circuit ~~digital processing system~~ in accordance with claim 10, wherein the address translation filter further comprises:

an output control link responsive to the refresh logic unit and operable to send a refresh signal the core processor when the translation lookaside buffer is to be refreshed.

12. (currently amended) An integrated circuit ~~digital processing system~~ in accordance with claim 10, wherein the core processor is operable to refresh the translation lookaside buffer when a refresh signal is received from the address translation filter.

13. (currently amended) An integrated circuit ~~digital processing system~~ in accordance with claim 12, wherein the translation lookaside buffer is refreshed via the system bus.

14. (currently amended) A digital processing system ~~in accordance with claim 9~~ comprising:

a core processor;

an external memory unit;

an external processing device;

an address translation filter; and

a system bus linking the core processor, the external memory and the address translation filter to each other and linking the external processing device to the address translation filter,

wherein the address translation unit is operable to translate a virtual memory address received via the system bus from the external processing device into a physical memory address transmitted via the system bus to the external memory unit and, wherein the bus is one of an AMBA bus and an AHB bus.

15. (currently amended) A method of memory address translation in an integrated circuit bus coupled between a core processor in the integrated circuit and [[the]] an external memory unit, the method comprising:

receiving a first bus signal from a device in the integrated circuit via the bus in accordance with a first bus protocol;

translating a virtual memory address specified by the first bus signal to a physical memory address in an address translation filter in the integrated circuit; and

transmitting a second bus signal via the bus to the external memory unit in accordance with ~~the physical memory address~~ a second bus protocol, the second bus signal specifying the physical memory address,

wherein the first bus protocol is the same as the second bus protocol.

16. (original) A method in accordance with claim 15, wherein the translating comprises:

selecting a physical memory address from a table of physical memory addresses, the table of physical memory addresses being indexed by virtual addresses.

17. (original) A method in accordance with claim 16, further comprising:

refreshing the table of physical memory addresses if the table has no entry for the virtual address.

18. (previously presented) A method in accordance with claim 17, wherein the refreshing comprises receiving data via the bus from the core processor coupled to the bus.

19. (previously presented) A method in accordance with claim 17, wherein the refreshing comprises:

signaling the core processor that the table of physical memory addresses needs to refreshed;

passing the virtual memory address to the core processor; and

receiving a new physical memory address from the core processor.

20. (original) A method in accordance with claim 17, wherein the first bus signal is received from a processing device, further comprising:

providing a system clock signal to the processing device; and

pausing the system clock signal while the table of physical memory

addresses is being refreshed.

21. (previously presented) A method in accordance with claim 15, wherein the second bus signal is transmitted to the external memory unit.

22. (original) A method in accordance with claim 15, wherein the first bus signal is received from a processing device.

23. (original) A method in accordance with claim 22, further comprising:

transferring code from a core processor to the processing device; and

transferring an initial memory map from the core processor to the address translation filter.

24. (new) A digital processing system in accordance with claim 9, wherein the bus is one of an AMBA bus and an AHB bus.

25. (new) A digital processing system in accordance with claim 14, wherein the address translation filter comprises:

a translation lookaside buffer; and

a refresh logic unit operable to refresh the translation lookaside buffer when the virtual memory address is not matched by an entry in the translation lookaside buffer.

26. (new) A digital processing system in accordance with claim 25, wherein the address translation filter further comprises:

an output control link responsive to the refresh logic unit and operable to send a refresh signal the core processor when the translation lookaside buffer is to be refreshed.

27. (new) A digital processing system in accordance with claim 26, wherein the core processor is operable to refresh the translation lookaside buffer when a refresh signal is received from the address translation filter.

28. (new) A digital processing system in accordance with claim 27, wherein the translation lookaside buffer is refreshed via the system bus.

29. (new) A digital processing circuit, comprising:

a core processor;

a processing device external to the core processor;

a system bus coupled to the core processor and operable to link the core processor to an external memory unit under a system bus protocol;

an address translation filter operable to couple the processing device to the system bus under the same system bus protocol,

wherein the address translation unit is operable to translate a virtual memory address received via the system bus from the processing device into a physical memory address, in the external memory, transmitted via the system

bus to the external memory unit.

30. (new) A digital processing circuit in accordance with claim 29, wherein the core processor, the address translation filter and the processing device occupy the same integrated circuit.

31. (new) A digital processing system in accordance with claim 29, wherein the system bus has an Advanced Micro-controller Bus Architecture.